Séminaire ASTRE : Fabrice Muller

27 Juin 2013, 10:00 – 11:30

Titre du séminaire et orateur

Le flot de conception FORTRESS.
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Date et lieu

Jeudi 27 juin 2013, 10h.
ENSEA, salle 384.

Abstract

FoRTReSS is an academic research project. It is a tool suite providing the user a way to explore the partial reconfiguration design space and ultimately proposing a set of reconfigurable regions and processors that will ensure a certain quality of service for a given application. FoRTReSS can be integrated into existing PR flows. It is placed between the synthesis phase, where all reconfigurable modules are synthesized into netlists, and the implementation phase, where the floorplan is created. FoRTReSS takes as an input netlists, synthesis reports and the targeted device from the first step. It also needs some more information about the application, in the form of a Control Data Flow Graph (CDFG) and additional timing information (e.g. execution times and deadline). To validate a solution, FoRTReSS relies on a SystemC simulator, called RecoSim. The flow is modular and each step can be customized in order to facilitate design space exploration by the designer.

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