Séminaire ETIS : Bane Vasic

05 Juin 2018, 11:00 – 12:00

Titre du séminaire et orateur

Improving Convergence of Iterative Decoders using Neural Networks.

Bane Vasic, University of Arizona.

Date et lieu

Mardi 5 juin 2018, 11h.

Université de Cergy-Pontoise, site de St-Martin 2, espace des colloques.

Abstract

In this talk, we discuss the perspectives of utilizing deep neural networks (DNN) to decode Low-Density Parity Check (LDPC) codes. The main idea is to build a neural network to learn and optimize a conventional iterative decoder of LDPC codes. A DNN is based on Tanner graph, and the activation functions emulate message update functions in variable and check nodes. We impose a symmetry on weight matrices which makes it possible to train the DNN on a single codeword and noise realizations only. Based on the trained weights and the bias, we further quantize messages in such DNN-based decoder with 3-bit precision while maintaining no loss in error performance compared to the min-sum algorithm. We use examples to present that the DNN framework can be applied to various code lengths. The simulation results show that, the trained weights and bias make the iterative DNN decoder converge faster and thus achieve higher throughput at the cost of trivial additional decoding complexity.

Short bio

Dr. Bane Vasic is a Professor of Electrical and Computer Engineering and Mathematics at the University of Arizona and a Director of the Error Correction Laboratory. He is an inventor of the soft error-event decoding algorithm, and the key architect of a detector/decoder for Bell Labs data storage read channel chips which were regarded as the best in industry. His pioneering work on structured low-density parity check (LDPC) error correcting codes and invention of codes has enabled low-complexity iterative decoder implementations. Structured LDPC codes are today adopted in a number of communications standards and data storage systems. Dr. Vasic is known for his theoretical work in error correction coding theory and codes on graphs which has led to characterization of the hard decision iterative decoders of LDPC codes, and design of decoders with best error-floor performance known today. He is a co-founder of Codelucida, a startup company developing advanced error correction solutions for communications and data storage. He is an IEEE Fellow, Fulbright Scholar, da Vinci Fellow, and a past Chair of IEEE Data Storage

Technical Committee.